REMARKS

Claims 1 – 20 remain pending in the present Application.

Objections

The present Office Action objects to Figure 1 reference to a "system master (SM) buss controller". Applicant has submitted a drawing amendment concurrently with the present response.

102 Rejections

Claims 1 – 3 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Schieve (US Patent 6,018,808). Applicant respectfully asserts that the present invention as recited in Claims 1 – 3 and 7 are neither shown nor suggested by the Schieve reference.

Applicant respectfully asserts that the Schieve reference is not directed to the present invention as recited in Claim 1. Specifically the present invention, as set forth in independent Claim 1 recites in part:

... processor configured to ... perform multi-tasking operations while accessing serial presence detect information during boot up operations prior to completing volatile memory initialization.

To the extent the reference may mention a master handler causes the storing of pertinent information relative to that which a microprocessor had been working when the interrupt occurred [Colum 4 lines 40-44], Applicant respectfully asserts the Schieve reference does not teach performing multi-tasking operations while accessing serial presence detect information during boot up operations. Applicant also respectfully asserts the present Office Action acknowledges Schieve fails to disclose a multi-tasking bootstrap system wherein the system management bus communicates serial presence detect data in an interrupt mode (page 7 second paragraph of present Office Action).

Applicant respectfully asserts Claims 1 - 7 are allowable as depending from an allowable independent Claim.

Claims 8-9 and 11-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Skrovan et al. (US Patent 6,016554). Applicant respectfully asserts that the present invention as recited in Claims 8–9 and 11-17 are neither shown nor suggested by the Skrovan et al. reference.

Applicant respectfully assert that the Skrovan et al. reference is not directed to the present invention as recited in Claim 8. Specifically the present invention, as set forth in independent Claim 1 recites in part:

...interrupt vector table information stored in a non volatile memory;...

programming a system management bus controller; and

operating said system management bus controller in a multitasking environment in which said system management bus controller operates in an interrupt driven mode prior to completing volatile memory initialization.

To the extent the Skrovan et al. reference may mention a memory model 16 implemented in software includes a memory control unit which includes a control signal generator 24 [Col. 3 lines 9-11], Applicant respectfully asserts the Skrovan et al. reference does not teach operating a system management bus controller in a interrupt driven mode in a multitasking environment. Applicant respectfully asserts software models running on a system that has already booted up do not teach boot up operations.

Applicant respectfully asserts Claims 8 - 17 are allowable as depending from an allowable independent Claim 8.

103 REJECTIONS

The present Office Action indicates Claims 4-6 and 18-20 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Shrieve (US Patent 6,018,808) in view of Skrovan et al. (US Patent 6,016,554). Applicant respectfully asserts that the present invention is neither shown nor suggested by the Shrieve nor Skrovan et al. references, alone or together.

Applicant respectfully assert that the Shrieve reference is not directed to the present invention as recited in Claim 18. As set forth above, Applicant respectfully asserts that the present invention is neither shown nor suggested by the Shrieve reference. The present Office Action acknowledges the Shrieve reference fails to disclose programming a system management bus controller, and operating the system management bus controller in a multitasking environment in which the system management bus controller operates in an interrupt driven mode prior to completing volatile memory initialization, wherein operating the system management bus controller includes retrieving serial presence detect data.

Applicant respectfully asserts the Skrovan reference does not overcome these and other shortcomings of the Shrieve reference. As set forth above To the extent the Skrovan et al. reference may mention a memory model 16 implemented in software includes a memory control unit which includes a control signal generator 24 [Col. 3 lines 9-11], Applicant respectfully asserts the Skrovan et al. reference does not teach operating a system management bus controller in a interrupt driven mode in a multitasking environment. Applicant respectfully asserts software models running on a system that has already booted up do not teach boot up operations.

Applicant respectfully asserts Claims 19 - 20 are allowable as depending from an allowable independent Claim 18.

CONCLUSION

In light of the above-listed amendments and remarks, Applicant respectfully requests allowance of the remaining Claims. The examiner is urged to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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